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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,313	04/16/2004	Bruce C. S. Chou	3722-0190PUS1	7759

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EXAMINER	
TERESINSKI, JOHN	

ART UNIT	PAPER NUMBER
2858	

DATE MAILED: 12/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/825,313	CHOU ET AL.	
	Examiner	Art Unit	
	John Teresinski	2858	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/16/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 9 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,587,343 to Kano et al..

Regarding claim 1, Kano et al. disclose a semiconductor sensor device and method having a substrate structure (column 4 lines 6-7), and a protection layer covering over the substrate structure, wherein the protection layer comprises, from bottom to top: a first layer for providing a first stress against the substrate structure; a second layer for providing a second stress against the substrate structure; and a third layer for providing a third stress against the substrate structure (column 4 lines 13-24), wherein the first stress and the third stress belong to one of a tensile stress/beam deformation due to curvature (column 6 lines 64-67), and the second stress belongs to compressive stress/stress relieving layer between the layers/films formed (column 2 lines 44-48, 61-67).

Regarding claim 9, Kano et al. disclose a protection layer with a thickness greater than 2 microns (column 4 lines 13-22).

Regarding claim 11, Kano et al. disclose a silicon substrate having a plurality of sense circuits and a plurality of sense electrodes (12,13), which is arranged in an array on the silicon

substrate, corresponds to the sense circuits, and electrically connected to the sense circuits, respectively (column 4 lines 34-49).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kano et al. in view of applicant's admitted prior art.

Regarding claim claims 2 and 3, Kano et al. disclose a first and third layer made of a poly crystalline silicon layer and the second layer made of silicon oxide (column 4 lines 13-22). Kano et al. does not disclose the first and second layer made of silicon dioxide with the second layer made of silicon nitride or silicon carbide, or the first and second layer made of silicon nitride or silicon carbide with the second layer made of silicon dioxide. Applicant's admitted prior art discloses a first and third layer made the first and second layer made of silicon dioxide with the second layer made of silicon nitride (page 3 lines 1-9). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include the specific materials as taught by applicants admitted prior art into the sensor of Kano et al. for the purpose of providing a sensor composed of a protection layer with good mechanical strength (page 3 lines 9-10). Further with respect to the rearrangement of layers as described in claim 3, it would have been obvious to one having ordinary skill in the art at the time the invention was made to , since it has

been held that rearranging parts of an invention involves only routine skill in the art. In re Japikse, 86 USPQ 70 C (CCPA 1950).

Claims 4-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kano et al. in view of U.S. Patent No. 6,686,227 to Zhou et al..

Regarding claims 4 and 5, Kano et al. does not disclose a polymeric material or ceramic atomic layer applied onto the third layer to provide a hydrophobic and lipophobic surface, which is to be in contact with a finger, so as to prevent a latent fingerprint from being formed thereon wherein the polymeric material layer is made of Teflon or Teflon-like chemical structure material. Zhou et al. disclose a method and system for molding integrated circuit packaging including a polymeric material applied onto upper surface, which is to be in contact with a finger, so as to prevent a latent fingerprint from being formed thereon wherein the polymeric material layer is made of Teflon or Teflon-like chemical structure material (column 3 lines 37-46). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a Teflon like layer as taught by Zhou et la. Into Kano et al. for the purpose of providing a means for preventing buildup on a sensor surface rendering measurements inaccurate.

Regarding claims 6 and 7, Kano et al. disclose a polar silane group is for firmly fixing the polymeric material layer to the third layer wherein the FC polymer end has a soft fragment FC polymer bond (column 4 lines 13-23).

Regarding claim 8, Kano et al. disclose ceramic atomic layer is an aluminum oxide layer (column 13 lines 36-44).

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kano et al..

Regarding claim 10, Kano et al. discloses the claimed invention except for the protective layer in the range of 3-5 microns. It would have been obvious to one having ordinary skill in the art at the time the invention was made to tailor the protective layer to a value in the range of 3-5 microns, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Claims 12- 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kano et al. in view of U.S. Patent No. 6,603,192 to Thomas et al..

Regarding claims 12, 13 and 16, Kano et al. disclose the device and method above but fails to teach a metal mesh crisscrossing between sense electrodes, being flush with the sense electrodes, and surrounding each of the sense electrodes, wherein the metal mesh is connected to a ground, and the protection layer completely covers over the metal mesh or ESD units connected to the metal mesh wherein the number of the ESD units is smaller than that of sense electrodes. Thomas et al. a method and device for passivition of a capacitive circuit including a metal mesh/grid crisscrossing between sense electrodes, being flush with the sense electrodes, and surrounding each of the sense electrodes, wherein the metal mesh is connected to a ground, and the protection layer completely covers over the metal mesh (column 4 lines 40-54) and ESD units connected to the metal mesh wherein the number of the ESD units is smaller than that of sense electrodes (column 4 lines 48-54). It would have been obvious to one of ordinary skill in

the art at the time the invention was made to include a metal mesh and ESD units as taught by Thomas et al. into Kano et al. for the purpose of improving scratch resistivity (column 1 lines 59-63).

Regarding claim 14, Kano et al. disclose a plurality of bonding pads serving as input/output portions of the chip-type sensor, wherein the protection layer partially covers over the bonding pads so as to form a plurality of first openings above the ESD units and a plurality of second openings above bonding pads, and a dimension of each of the first openings is smaller than that of each of the second openings (column 11 lines 35-65).

Regarding claim 15, Kano et al. in view of Thomas et al. disclose the claimed invention except for a spacing between two adjacent ESD units substantially ranges from 500 to 1000 microns. It would have been obvious to one having ordinary skill in the art at the time the invention was made to tailor the protective layer to a value in the range of 500 to 1000 microns, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John Teresinski whose telephone number is (571) 272-2235. The examiner can normally be reached on M-F 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Diane Lee can be reached on (571) 272-2399. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JT
JT
November 29, 2005

ANJAN DEB
PRIMARY EXAMINER